

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Richard A. Blanchard et al.

Appln No.: 10/712,810

Filed: 11/13/2003

Title: METHOD FOR FABRICATING A POWER SEMICONDUCTOR DEVICE HAVING A VOLTAGE SUSTAINING LAYER WITH A TERRACED TRENCH FACILITATING FORMATION OF FLOATING ISLANDS

Art Unit: 2814

Examiner: Thao X. Le

Confirm. No.: 8845

Docket No.: GS 160 D1

Via Facsimile 571-273-2885
Mail Stop Issue Fee
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Sir:

This is filed in response to the Examiner's statement of reasons for allowance which were set forth in connection with the Notice of Allowance mailed July 20, 2007. These comments are being filed simultaneously with the payment of the government issue fee.

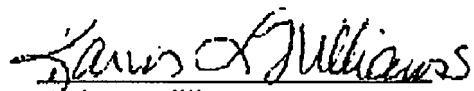
The Examiner's statement of reasons for allowance indicates claims 24-41 are allowed because the prior art of record neither anticipates nor renders obvious the limitations of the base claims 24-27 and, the Examiner states a partial recitation of elements of independent Claims 24-27.

**Application SN
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Applicant respectfully submits that it is the complete recitation of all of the elements recited in *each* of the individual pending claims, Claims 24-41 (including independent Claims 24-27), that constitute the basis for allowance for each allowed claim.

Applicant's undersigned attorney may be reached at (908) 518-7700.

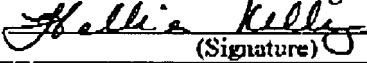
Respectfully submitted,


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I hereby certify that this document and any document referenced herein is being sent to the United States Patent and Trademark office, Mail Stop Issue Fee, via Facsimile to: 571-273-2885 on 10/22/07.

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